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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,368	04/29/2004	Eric Chuang	VIAP0106USA	3367

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EXAMINER
VO, THANH DUC

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 05/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,368	CHUANG ET AL.	
	Examiner	Art Unit	
	Thanh D. Vo	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 10-15* is/are rejected.

7)☒ Claim(s) *2-9 and 16-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Application filed on April 29, 2004. Claims 1-20 are presented for examination. Claims 1-20 are pending.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 10, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Date et al. (US 6,499,076).

As per claim 1, Date et al. discloses a method of controlling data transmission within a memory of a computer system, the computer system comprising a processor (col. 7, lines 50-51), and a memory controller (col. 7, lines 50-51, DMA controller) connected to the processor and the memory, the method comprising the following steps:

a) delivering a plurality of data located in a plurality of first memory addresses of the memory to the memory controller (col. 1, lines 27-28, *wherein the memory controller reads the data from the memory which inherently comprising of memory addresses*); and

b) the memory controller directly storing the plurality of data in a plurality of second memory addresses of the memory instead of transmitting the plurality of data to the processor. See col. 1, lines 28-30, *wherein the DMA processed the data then write it back to the memory and further inherently comprising of memory addresses.*

As per claim 10, Date et al. discloses a computer system comprising:

a processor (col. 7. lines 47-51) for controlling operations of the computer system;

a memory comprising a plurality of first memory addresses and a plurality of second memory addresses (col. 6, lines 61-62, *wherein a memory comprises of plurality of memory addresses and the memory addresses are different from each other, therefore the memory addresses can be virtually viewed as lower (first) address regions and upper (second) address region*); and

a memory controller (col. 7, lines 50-52) electrically connected to the processor and the memory, the memory controller having an internal data transmission controller for retrieving a plurality of data according to the first memory addresses, and directly storing the plurality of data in the second memory addresses instead of transmitting the plurality of data to the processor (col. 1, lines 27-32, *wherein the memory controller has*

read/write capability therefore it is equivalent to a transmission controller since transmission is a method of transferring the data including read and write).

As per claim 11, Date disclosed a computer system wherein the memory controller further comprises:

an address register for receiving the first memory addresses and the second memory addresses, *wherein an address register has to be existed in any hardware system of Date et al. in order to hold or temporarily store the data content to be transferred or copied to another location or compared with another data content*; and

a data register is also an inherent feature in hardware system in order for storing the data to be transferred the content being held in the register or compared with the other data being held in another data register.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Date et al. (US 6,499,076) in view of Burton (US 2004/0088467).

As per claim 12, Date et al. did not particularly disclose a computer system wherein the memory controller is installed in a north bridge circuit.

Burton disclosed a memory controller is installed in a north bridge circuit (Fig. 1, item 102, page 1, paragraph 0007, lines 1-3).

It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to implement a memory controller within a north bridge circuit since the north bridge circuit is directly coupled to the system memory. Therefore, having a memory controller installed in a north bridge would enhance the data transmission rate and saving circuit area.

5. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Date et al. (US 6,499,076) in view of Lee et al. (US 2003/0088742).

As per claim 13, Date et al. did not particularly disclose a computer system wherein the memory comprises a display memory and a system memory.

Lee et al. teaches a memory wherein the memory comprises of system memory and graphic frame buffer memory. See page 1, paragraph 0004, lines 3-5.

It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the system of Date et al. and implement the memory teaches by Lee et al. since Date et al. has a DMA controller which is capable of directly processing the data transferred from the memory and writing the processed data back to the memory. Therefore, having a memory comprises of system memory and graphic

memory addresses will greatly enhanced the system speed and throughput since the DMA controller would be able to process both type of memory contents without the intervention from a processor.

As per claims 14 and 15, Lee et al. discloses a computer system wherein the first memory addresses are in the display memory and the second memory addresses are in the system memory. *It is readily apparent to one having an ordinary skill in the art at the time of the applicant's invention to recognize that the memory content is required to have a memory address in order to allocate and de-allocate its content. Therefore, display memory and system memory have to have their own memory addresses in order for the system to read and write the content belongs to each memory address.*

Allowable Subject Matter

6. Claims 2, 5, 16, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3-4, 6-9, and 18-20 are depending from allowable claims 2, 5, and 17, respectively. Therefore, they are also allowable.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

With respect to allowable dependent claims 2, 5, 16, and 17, the following prior art of record is considered pertinent to the applicant's disclosure.

Takahashi (US 2003/02066480) discloses a method of read and write to continuous address are transferring from a semiconductor memory wherein the bit length is sequentially output through a bi-directional interface. See claims 15 and 18.

Yagi et al. (US 2003/0046489) disclosed a method of transferring discontinuous data from a memory (page 3, paragraph 0027).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thanh Vo
Patent Examiner
AU 2189
05/01/2006

REGINALD G. BRAGDON
PRIMARY EXAMINER